

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 12 and 22 in accordance with the following:

1-11 (CANCELLED)

12. (CURRENTLY AMENDED) A thin film transistor (TFT), comprising:
a substrate;
a semiconductor layer formed over said substrate having end portions;
a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer;
a gate electrode formed over said first insulating layer;
a capping layer formed over said gate electrode;
spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer;
high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; and
source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions.

13. (PREVIOUSLY PRESENTED) The TFT of claim 12, further comprising low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers.

14. (ORIGINAL) The TFT of claim 12, wherein said first insulating layer, said capping layer and said spacer are one of an oxide layer and a nitride layer.

15. (ORIGINAL) The TFT of claim 12, further comprising a silicide layer formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

16. (ORIGINAL) The TFT of claim 15, wherein said silicide layer is of a refractory metal.

17-21 (CANCELLED)

22. (CURRENTLY AMENDED) An active matrix display device, comprising:
a substrate;
a semiconductor layer having end portions formed over said substrate;
a first insulating layer formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer;
a gate electrode formed over said first insulating layer;
a capping layer formed over said gate electrode;
spacers formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer;
high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers;
source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions;
a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes; and
a pixel electrode formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

23. (ORIGINAL) The active matrix display device of claim 22, further comprising low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers.

24. (ORIGINAL) The active matrix display device of claim 22, further comprising

silicide layers formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

25. (ORIGINAL) The active matrix display device of claim 22, further comprising an organic electro-luminescence (EL) layer and a cathode electrode sequentially formed on a first predetermined area of said pixel electrode and on a second predetermined area of said planarization layer.